and the Examiner points to I/O controller 221 of Gates' figure 2A as showing that the signals are generated using an I/O controller of the host adapter. Lastly the Examiner reads the step of electronically selecting PCI signal lines as taught by Gates at column 41, lines 41-42 and the step of assessing timing of the generated signals as Gates' table 14A (also in column 41).

With due respect, Applicant takes issue with much of the Examiner's reading of the recited steps as taught in Gates. Admittedly Gates teaches a circuit that includes some self-test capabilities and features. Of course this broad concept is not that which the Applicant claims as his invention. Beyond broadly teaching a host adapter that includes some self test features, Applicant respectfully disagrees with the Examiner's assertions that the claimed features of, for example, claim 1 are taught by Gates.

First, the Examiner suggests that the step of "generating PCI signals" is in some manner taught by support circuit 250 of figure 2A (et. seq.). Nothing of the sort is taught by element 250 of figure 2A of Gates. The broad purpose of support circuit 250 is to remove various tangential functions from the core host bus adapter function of circuit 240. The tangential features so removed are embodied in the features of support circuit 250 coupled to the host bus adapter 240 by a 1-bit wide serial interface 241. Thus, functions that previously may have consumed significant numbers of I/O pins/pads on the circuit die of the host bus adapter 240 may be removed to the support circuit 250. The reduced I/O pin/pad count of the host bus adapter circuit 240 allows more "real estate" in the circuit design for more complex processing functions. Less important features such as LED management for user interaction etc. are relegated to the support circuit 250. Only a single pin 241 is required of the host bus adapter 240 to provide the interface to the support circuit 250. Gates explains the broad features of the separation of features in his supporting text at column 5, line 2 through column 7, line 37.

The Examiner's assertion that step of "generating PCI signals" is somehow taught by the presence of support circuit 250 is simply unfounded. One of ordinary skill in the art would find no teaching or suggestion of such a step in the structure or operation of the system of Gates' figure 2A or any of the associated descriptive text or supporting figures.

Still further, the Examiner next reads the requirement of claim 1 that the step of "generating PCI signals" uses an "I/O controller of the host adapter" as taught by controller 221 of Gates' figure 2A. This is inconsistent with the Examiner's earlier reading of the step of "generating PCI signals" as taught by support circuit 250 - separate and distinct from the host bus adapter circuit 240 of Gates' figure 2A. Thus for the same element, the Examiner appears to read the same element as both element 250 and element 221 without suggesting how either of the two element meets the recitation of generating PCI signals.

Next the Examiner reads the step in claim 1 of "electronically selecting one or more PCI signals" as Gates' text at column 41, lines 41-42. This cited passage reads in its entirety as follows: "input characteristics. Examples of timing characteristics are listed in Tables 14A-14C." Even including the preceding portion of the leading partial sentence the passage reads as follows: "So a serial port 230 that exhibits fast characteristics must output no faster than a slave serial port input-output circuit 254 that exhibits slow input characteristics. Examples of timing characteristics are listed in Tables 14A-14C." Applicant finds nothing in this cited passage that even remotely suggests a step of electronically selecting one or more of the PCI signals.

Lastly as regards rejected claim 1, the Examiner reads the step of "assessing timing of the one or more PCI signals" as Table 14A in Gates (in column 41 starting at about line 45). This table discusses typical timing of the signals exchanges on the single bit wide serial interface 241 between the host adapter circuit 240 and the support circuit 250 - i.e., between serial port 230 of host adapter 240 and serial port 254 of support circuit 250. These signals are not PCI signals, let alone the PCI signals electronically selected, let alone the PCI signals generated by a controller in the host adapter - all as required by the recitations of rejected claim 1. Still further, the cited Table 14A does not relate to a step of assessing the timing of generated signals but rather is a table suggesting desired typical timing for the serial interface provided by the teachings of Gates.

Nothing in the cited teachings of Gates teaches or even remotely suggests the recited steps of, for example, rejected claim 1. In particular, as discussed above, the steps

of generating PCI signals, electronically selecting one or more of the generated PCI signals, and assessing timing of the selected PCI signals is simply not taught or reasonably suggested to one of ordinary skill in the art by the teachings of Gates.

The Examiner similarly cites passages of Gates as teaching features of the rejected dependent claims (2-3 and 8-10) dependent from base claim 1. For example, the Examiner suggests that column 3, lines 59-63 teach the features of claim 2 wherein the step of electronically selecting includes using addresses within a memory of the adapter to select among the PCI signals. The cited teachings read (in their entirety) as follows:

> Instead of a slave serial port input-output circuit, a programmable logic circuit or a shift register can pass to the host adapter, for example, a device identification byte and byte of status of various resources accessible through the serial port.

Nothing in this passage would be understood by one of ordinary skill in the art to teach or even remotely suggest that the memory addresses are used in any manner to select a PCI signal for later timing assessment. Rather, this passage relates to the particular structures that may be employed for the 1-bit wide serial communication link (241) between the host adapter 240 and the support circuit 250. This passage merely points out that a standard serial controller may be employed as well as discrete logic including a shift register to implement the serial interface ports (e.g., 230 and 254) of Gates.

Or, for example, where rejected claim 3 recites that the information stored in the memory is addresses - addresses used in the step of electronically selecting PCI signals, the Examiner cites column 3, line 36 which reads (in context): "To read a four-byte word from an address in memory, such as a random-access-memory the serial port transmits a packet containing the command byte followed by two packets containing the address bytes and then waits for an acknowledge packet followed by four packets containing data bytes." Applicant is puzzled again as to how this teaching has anything to do with the recited element of storing addresses in a memory that is then used to electronically select PCI signals for later timing assessment.

In like manner, the Examiner cites column 3, lines 59-63 (as quoted above) for the teaching of the recited use in claim 8 of a logic analyzer to perform the recited step of assessing. The cited passage has nothing whatsoever to do with use of a logic analyzer to assess timing of selected PCI signals - it doesn't even mention a logic analyzer.

And again, in rejecting claim 10, where the step of assessing is recited as including assessing one or both of slew rate and clock-to-signal valid timing of the selected PCI signals, the Examiner points to Gates at column 41, lines 31-34 where Gates is discussing the clocking of serial bits exchanged over the serial interface 241 between the adapter 240 and the support circuit 250. As noted above, this 1-bit serial interface is not a PCI bus. Further, the cited passage is not discussing assessing the timing of any signals but rather providing exemplary timing requirements to enable the desired serial data transmission over link 241 of Gates.

The Examiner rejected independent claims 11 and 17 and all other dependent claims with similar spurious arguments and readings of the teachings of Gates. The Examiner has simply failed to apply the cited art in any manner that presents a prima facie case of anticipation or obviousness. The art of record simply does not teach or reasonably suggest the features of the invention as claimed. At best, the cited art is tangentially related in that it relates to aspects of a host bus adapter (and HBA) as does the subject application. But it does not even remotely address issues of dynamically selecting PCI signals by operation within the HBA and assessing timing of those selected PCI signals. Gates is simply unrelated to the claimed invention of the subject application

Applicant therefore maintains that all remaining claims are allowable over all art of record, considered individually or in any combination. Applicant respectfully requests reconsideration and withdrawal of the outstanding rejection and objection.

Conclusion

Applicant has thoroughly discussed the rejection of the claims and respectfully requests reconsideration and withdrawal of all outstanding rejections and objections.

LSI Docket No. 03-0376

No additional fees are believed due. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

Respectfully submitted,

Daniel N. Fishman #35,512
Duft Bornsen & Fishman, LLP
1526 Spruce Street, Suite 302
Boulder, CO 80302
(303) 786-7687
(303) 786-7691 (fax)